What Is Claimed Is:

1. An array substrate for a liquid crystal display device, comprising:

a substrate;

a data line over the substrate in a first direction;

a gate line over the substrate in a second direction perpendicular to the data line, so that the data and gate lines cross to each other to define a pixel region;

a thin film transistor disposed near a crossing of the data and gate lines, the thin film transistor comprising:

source and drain electrodes over the substrate;

an active layer over the source and drain electrodes;

an ohmic contact layer between the active layer and the source electrode and between the active layer and the drain electrode;

a gate insulation layer over the active layer; and

a gate electrode over the gate insulation layer;

a black matrix over the thin film transistor and over the data line, the black matrix exposing a portion of the drain electrode;

a color filter disposed over the substrate within the pixel region, the color filter covering a portion of the drain electrode and exposing another portion of the drain electrode; and

a pixel electrode over the color filter within the pixel region, the pixel electrode contacting an exposed portion of the drain electrode.

2. The array substrate of claim 1, further comprising:

a storage capacitor that includes a storage metal layer, a portion of the gate line, and an insulating pattern interposed between the storage metal layer and the gate line; and

doped and pure amorphous silicon patterns between the storage metal layer and the insulating pattern;

wherein the pixel electrode electrically contacts a portion of the storage metal layer.

4. The array substrate of claim 2, wherein the data line, the source electrode, the drain electrode and the storage metal layer are formed during the same mask process using identical material selected from the group consisting of chromium (Cr), molybdenum (Mo), tungsten (W), titanium (Ti), copper (Cu), aluminum (Al) and an aluminum alloy.

5. The array substrate of claim 2, wherein the gate insulation layer and the insulating pattern are formed of identical material selected from the group consisting of silicon nitride, silicon oxide and silicon oxynitride.

6. The array substrate of claim 1, wherein the color filter has one of red, green or blue colors and has a continuous color formation with next color filters formed in up-and-down directions.

7. An array substrate for a liquid crystal display device, comprising:

a substrate including a data region, a TFT region, a pixel region and a gate region;

a black matrix over the substrate corresponding to the data region and the TFT region;

a buffer layer over the substrate to cover the black matrix;

a data line over the buffer layer in a first direction, the data line corresponding to the data region;

a gate line over the buffer layer corresponding to the gate region in a second direction perpendicular to the data line, wherein the data and gate lines cross to each other, thereby defining the pixel region;

a thin film transistor disposed over the buffer layer near a crossing of the data and gate lines, the thin film transistor corresponding to the TFT region and comprising:

source and drain electrodes over the buffer layer;

an active layer over the source and drain electrodes;

an ohmic contact layer between the active layer and the source electrode and between the active layer and the drain electrode;

a gate insulation layer over the active layer; and

a gate electrode over the gate insulation layer;

a color filter disposed over the buffer layer within the pixel region, the color filter covering a portion of the drain electrode while exposing another portion of the drain electrode; and

a pixel electrode over the color filter within the pixel region, the pixel electrode contacting an exposed portion of the drain electrode.

8. The array substrate of claim 7, further comprising:

a storage capacitor that includes a storage metal layer, a portion of the gate line, and an insulating pattern interposed between the storage metal layer and the gate line; and

doped and pure amorphous silicon patterns between the storage metal layer and the insulating pattern;

wherein the pixel electrode electrically contacts a portion of the storage metal layer.

9. The array substrate of claim 8, wherein the data line, the source electrode, the drain electrode and the storage metal layer are formed in the same mask process using identical material selected from the group consisting of chromium (Cr), molybdenum (Mo), tungsten (W), titanium (Ti), copper (Cu), aluminum (Al) and an aluminum alloy.

10. The array substrate of claim 8, wherein the gate insulation layer and the insulating pattern are formed of identical material selected from the group consisting of silicon nitride, silicon oxide and silicon oxynitride.

11. The array substrate of claim 7, wherein the color filter has one of red, green or blue colors and has a continuous color formation with next color filters formed in up-and-down directions.

12. The array substrate of claim 7, wherein the buffer layer comprises at least one material selected from the group consisting of silicon nitride, silicon oxide and silicon oxynitride.

13. A method of fabricating an array substrate for a liquid crystal display device, comprising:

forming a first metal layer and a doped amorphous silicon layer in series over a substrate;

patterning the first metal layer and the doped amorphous silicon layer simultaneously to form a data line, a source electrode and a drain electrode;

forming a pure amorphous silicon layer, an insulating layer and a second metal layer in series over the substrate to cover the data line, the source electrode and the drain electrode;

patterning the pure amorphous silicon layer, the insulating layer and the second metal layer simultaneously to form an active layer, a gate insulation layer, a gate electrode and a gate line, thereby forming a thin film transistor comprising the source and drain electrode, the active layer and the gate electrode, wherein the gate line perpendicularly crosses the data line to form a pixel region;

forming a black matrix over the thin film transistor and on the data line, except for a portion of the drain electrode;

forming a color filter over the substrate within the pixel region, the color filter covering a portion of the drain electrode with exposing another portion of the drain electrode; and

forming a pixel electrode over the color filter within the pixel region, the pixel electrode contacting an exposed portion of the drain electrode.

14. The method of claim 13, wherein patterning the first metal layer and the doped amorphous silicon layer forms a storage metal layer over the substrate.

15. The method of claim 14, wherein patterning the pure amorphous silicon layer, the insulating layer and the second metal layer forms a doped amorphous silicon pattern, a pure amorphous silicon pattern and an insulating pattern in series between the storage metal layer and the gate line.

16. The method of claim 15, wherein the storage metal layer, a portion of the gate line and the insulation pattern comprise a storage capacitor.

17. The method of claim 14, wherein the pixel electrode electrically contacts a portion of the storage metal layer.

18. The method of claim 13, wherein the first metal layer comprises at least one metallic material selected from the group consisting of chromium (Cr), molybdenum (Mo), tungsten (W), titanium (Ti), copper (Cu), aluminum (Al) and an aluminum alloy.

19. The method of claim 13, wherein the insulation comprises at least one material selected from the group consisting of silicon nitride, silicon oxide and silicon oxynitride.

20. The method of claim 13, wherein the color filter has one of red, green or blue colors and has a continuous color formation with next color filters formed in up-and-down directions.

21. The method of claim 13, wherein the black matrix comprises a photosensitive black resin.

22. A method of fabricating an array substrate for a liquid crystal display device, comprising:

defining a data region, a TFT region, a pixel region and a gate region in a substrate;

forming a black matrix over the substrate corresponding to both the data region and the TFT region;

forming a buffer layer over the substrate to cover the black matrix;

forming a data line over the buffer layer in a first direction, the data line corresponding to the data region;

forming a gate line over the buffer layer to correspond to the gate region in a second direction perpendicular to the data line, wherein the data and gate lines cross each other, thereby defining the pixel region;

forming a thin film transistor over the buffer layer near the crossing of the data and gate lines, the thin film transistor corresponding to the TFT region and comprising:

source and drain electrodes over the buffer layer;

an active layer over the source and drain electrodes;

an ohmic contact layer between the active layer and the source electrode and between the active layer and the drain electrode;

a gate insulation layer over the active layer; and

a gate electrode over the gate insulation layer;

forming a color filter over the buffer layer within the pixel region, the color filter covering a portion of the drain electrode while exposing another portion of the drain electrode; and

forming a pixel electrode over the color filter within a pixel region, the pixel electrode contacting an exposed portion of the drain electrode.

23. The method of claim 22, further comprising forming a storage capacitor that includes a storage metal layer, a portion of the gate line, and an insulating pattern interposed between the storage metal layer and the gate line.

24. The method of claim 23, wherein the pixel electrode electrically contacts a portion of the storage metal layer.

25. The method claim 23, further comprising forming doped and pure amorphous silicon patterns between the storage metal layer and the insulating pattern.

26. The method of claim 23, wherein the data line, the source electrode, the drain electrode and the storage metal layer are formed in the same mask process using identical material selected from the group consisting of chromium (Cr), molybdenum (Mo), tungsten (W), titanium (Ti), copper (Cu), aluminum (Al) and an aluminum alloy.

27. The method of claim 23, wherein the gate insulation layer and the insulating pattern are formed of identical material selected from the group consisting of silicon nitride, silicon oxide and silicon oxynitride.

28. The method of claim 22, wherein the color filter has one of red, green or blue colors and has a continuous color formation with next color filters formed in up-and-down directions.

29. The method of claim 22, wherein the buffer layer comprises at least one material selected from the group consisting of benzocyclobutene (BCB), acrylic resin, methacrylic resin, silicon nitride, silicon oxide and silicon oxynitride.

30. The method of claim 22, the black matrix is one of a single layer of chromium or a double layer of chromium and chromium oxide.

31. A liquid crystal display device, comprising:

first and second substrates spaced apart from each other;

a data line over the first substrate in a first direction;

a gate line over the first substrate in a second direction perpendicular to the data line, so that the data and gate lines cross to each other to define a pixel region;

a thin film transistor disposed over the first substrate near a crossing of the data and gate lines, the thin film transistor comprising:

source and drain electrodes over the first substrate;

an active layer over the source and drain electrodes;

an ohmic contact layer between the active layer and the source electrode and between the active layer and the drain electrode;

a gate insulation layer over the active layer; and

a gate electrode over the gate insulation layer;

a color filter disposed over the first substrate within the pixel region, the color filter covering a portion of the drain electrode with exposing another portion of the drain electrode;

a pixel electrode over the color filter within the pixel region, the pixel electrode contacting an exposed portion of the drain electrode;

a black matrix over the second substrate, the black matrix corresponding to both the data line and the thin film transistor; and

a common electrode over an entire of the second substrate to cover the black matrix.